WE CLAIM:

1. An apparatus for implementing a high-availability computer system architecture, comprising:

a physical pipe for transferring data between an active computer system and a standby computer system;

a first logical pipe for transferring data over the physical pipe; and

a second logical pipe for transferring high-availability data over the physical pipe.

2. The apparatus of claim 1, wherein the data transferred between the active computer system and the standby computer system on the first logical pipe comprises checkpointing data.

3. The apparatus of claim 1, wherein the high-availability data transferred between the active computer system and the standby computer system on the second logical pipe comprises total system state data of the active computer system.

4. The apparatus of claim 1, wherein the second logical pipe uses remote direct memory access write operations for transferring high-availability data.

5. The apparatus of claim 1, wherein the second logical pipe uses remote direct memory access read operations for transferring high-availability data.

6. An apparatus for implementing a high-availability computer system architecture, comprising:

a physical pipe for transferring data between an active computer system and a standby computer system; and

a network interface card for transferring data and high-availability information over the physical pipe.

7. The apparatus of claim 6, wherein the data transferred between the active computer system and the standby computer system on the network interface card comprises checkpointing data.

8. The apparatus of claim 6, wherein the high-availability information transferred between the active computer system and the standby computer system on the network interface card comprises total system state data of the active computer system.

9. The apparatus of claim 6, wherein the second logical pipe uses remote direct memory access write operations for transferring high-availability data.

10. The apparatus of claim 6, wherein the second logical pipe uses remote direct memory access read operations for transferring high-availability data.

11. A system for implementing a high-availability computer system architecture, comprising:

a physical pipe;

an active computer system for transferring data and high-availability information over the physical pipe; and

a standby computer system for receiving the high-availability information from the physical pipe.

12. The system according to claim 11, wherein the active computer system further comprises:

an interface card for transferring the data and high-availability information.

13. The system according to claim 11, wherein the standby computer system further comprises:

an interface card for receiving the high-availability information.

14. A system for implementing a high-availability computer system architecture, comprising:

physical means for transferring data between an active computer system and a standby computer system;

a first logical means for transferring data over the physical means; and

a second logical means for transferring high-availability data over the physical means.

15. The system of claim 14, wherein the data transferred between the active computer system and the standby computer system on the first logical means comprises checkpointing data.

16. The system of claim 14, wherein the high-availability data transferred between the active computer system and the standby computer system on the second logical means comprises total system state data of the active computer system.

17. The system of claim 14, wherein the second logical means uses remote direct memory access read and write operations for transferring high-availability data.

18. An apparatus for implementing a high-availability computer system architecture, comprising:

a physical pipe for transferring data between an active computer system and a standby computer system;

a first logical pipe for transferring checkpointing data over the physical pipe; and

a second logical pipe for transferring total system state data over the physical pipe.

19. The apparatus of claim 18, wherein the second logical pipe uses remote direct memory access write operations for transferring total system state data over the physical pipe.

20. The apparatus of claim 18, wherein the second logical pipe uses remote direct memory access read operations for transferring total system state data over the physical pipe.

21. A method in a high-availability computer system having an active computer system and a standby computer system, the method comprising the steps of:

sending a message to the standby computer system to enter a switch-over state;

monitoring a transfer complete marker;

transferring total system state from the active computer system to the standby computer system; and

switching from the active computer system to the standby computer system upon detecting the transfer complete marker.

22. The method of claim 21, wherein the step of transferring total system state from the active computer system to the standby computer system, further includes the step of:

performing remote direct memory access read and write operations.

23. A computer-readable medium containing instructions for performing a method in a high-availability computer system having an active computer system and a standby computer system, the method comprising the steps of:

sending a message to the standby computer system to enter a switch-over state;

monitoring a transfer complete marker;

transferring total system state from the active computer system to the standby computer system; and

switching from the active computer system to the standby computer system upon detecting the transfer complete marker.

24. The computer-readable medium of claim 23, wherein the step of transferring total system state from the active computer system to the standby computer system, further includes the step of:

performing remote direct memory access read and write operations.